

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Birdsley et al.	Examiner:	Wille, D.
Application No.:	09/755,008	Group Art Unit:	2814
Filed:	January 5, 2001	Docket No.:	AMDA.469PA (TT3943)
Title:	Optical Analysis of Integrated Circuits		

---

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on August 3, 2005.

By: Kelly S. Waltigny  
Kelly S. Waltigny

APPEAL BRIEF

Board of Patent Appeals and Interferences  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

Customer No.  
**40581**

Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. § 41.37 for the above-referenced patent application. Please charge Deposit Account No. 01-0365 (TT3943) in the amount of \$500.00 for this brief in support of appeal as indicated in 37 C.F.R. § 41.20(b)(2). If necessary, authority is given to charge/credit deposit account 01-0365 (TT3943) any additional fees/overages in support of this filing.

RECEIVED  
2005 AUG 10 PM 2:48  
BOARD OF PATENT APPEALS  
AND INTERFERENCES

## **I. Real Party in Interest**

The real party in interest is the assignee, Advanced Micro Devices, Inc.

## **II. Related Appeals and Interferences**

Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

## **III. Status of Claims**

Claims 12-20 are presented for appeal and each of the appealed claims, 12-20, is rejected. Claims 1-11 have been canceled. The pending claims under appeal, as presently amended, may be found in the attached Appendix of Appealed Claims.

## **IV. Status of Amendments**

No amendments were filed subsequent to the final Office Action dated March 15, 2005.

## **V. Summary of Invention**

The independent claims involved in the appeal are directed to an arrangement for performing post manufacture analysis of SOI flip chip dies having a buried oxide layer (BOX) in a manner that preserves the integrity of the dies. While using an optical beam to probe circuitry avoids this type of damage to dies due to substrate removal, intrusion of the optical beam into the SOI circuitry can result in disruption of the operation of, or other damage to, circuitry components. The instant invention avoids both types of damage to SOI flip chip dies by modulating the optical beam.

One embodiment of Appellant's invention is directed to an arrangement for analyzing an integrated circuit having a silicon on insulator (SOI) structure. *See, e.g.*, Fig. 2 and the corresponding discussion at page 8, line 15 – page 10, line 10. The arrangement includes a means for directing a modulated optical beam (*e.g.*, 120) at a selected portion of the SOI structure (*e.g.*, 15) where the modulation is adapted to inhibit optical beam intrusion upon the integrated circuit and means for obtaining a reflected optical waveform response (*e.g.*, Fig 3) from the SOI selected portion. The means for directing may include, for example, an IR laser as discussed at page 8, line 15 – page 9, line 15, and the means for obtaining a reflected

optical waveform response may include, for example, a computer arrangement 150, as discussed at page 10, lines 1-10.<sup>1</sup>

Another embodiment is directed to using a combination of an optical beam arrangement (*e.g.*, 110) and a detection arrangement (*e.g.*, 140) to formulate an arrangement for analyzing an integrated circuit having a silicon on insulator (SOI) structure (*e.g.*, 15). The optical beam arrangement is adapted to direct a modulated optical beam (*e.g.*, 120) at a selected portion of the SOI structure and to inhibit intrusion of the optical beam upon the integrated circuit via the modulation. The detection arrangement is adapted to detect a reflected optical waveform response (*e.g.*, Fig 3) from the SOI structure selected portion.

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

---

<sup>1</sup> Appellant notes that the two means limitations may optionally be implemented using the same tool. A single structural element may perform two functions and may support two different claim terms. *Reed v. Edwards*, 26 C.C.P.A. 901, 101 F.2d 550, 554, 40 USPQ 620, 622 (CCPA 1939); *In re Kelley*, 49 C.C.P.A. 1359, 305 F.2d 909, 914, 134 USPQ 397, 401 (CCPA 1962) (as cited in the unpublished decision of *Winbond Elec. Corp. v. Int'l. Trade Comm.*, 4 Fed.Appx. 832, 2001 WL80412 (Fed. Cir. Jan. 13, 2001)).

## **VI. Grounds of Rejection**

- A. Claims 12-20 are rejected under 35 U.S.C. § 112(2).**
- B. Claims 12-16, 18 and 19 are rejected under 35 U.S.C. § 103(a) over Paniccia *et al.* (U.S. Patent No. 6,072,179) in view of Kikuchi (U.S. Patent No. 5,999,006).**
- C. Claims 17 and 20 are rejected under 35 U.S.C. § 103(a) over Paniccia *et al.* in view of Kikuchi and further in view of Dickol *et al.* (U.S. Patent No. 5,381,421).**

## **VII. Argument**

- A. Claims 12-20 comply with 35 U.S.C. § 112(2), and the Examiner's rejection lacks logical support and ignores the evidence of record.**

The Examiner continues to allege that a certain aspect of the claimed invention is unpatentable because the Examiner wishes to know: (1) whether the modulation prevents the optical beam from reaching the circuit; or (2) whether the optical beam is of sufficiently short duration that the optical signal is not detected by the circuit. These questions are not relevant and are ambiguous, as the answer to both questions would depend on the context in which the Examiner is applying these questions. Under Section 112(2), the law requires that the claims set forth the subject matter that applicants regard as their invention; and that the claims particularly point out and distinctly define the metes and bounds of the subject matter that will be protected by the patent grant. Contrary to the Examiner's position, the law does not require a description of specific embodiments

Under Section 112(2), the real objective issue is whether the claims reasonably apprise one skilled in the art of the scope of the invention. The Examiner questions only the claim term "inhibit" from the clause: "directing a modulated optical beam at a selected portion of the SOI structure, the modulation being adapted to inhibit optical beam intrusion upon the integrated circuit." The evidence of record indicates that Appellant's Specification, and dictionary definitions support Appellant's use of the term "inhibit" in the context of "modulation being adapted to inhibit optical beam intrusion upon the integrated circuit."

Below, Appellant first addresses the Examiner's hypothetical questions and secondly addresses the evidence of record.

**1. The Examiner's continued rejection of claims 12-20 is not based the requirements of § 112(2) but rather is based on hypothetical questions that would attempt to describe the invention under certain unspecified conditions.**

Throughout the examination of the instant application, the Examiner has maintained two hypothetical questions: (1) whether the modulation prevents the optical beam from reaching the circuit; or (2) whether the optical beam is of sufficiently short duration that the optical signal is not detected by the circuit. The answers to both questions, are dependent upon the context of a specific embodiment and would differ, for example, with respect to the modulation timing (longer "on" or longer "off" periods) and the material being optically probed (the bulk silicon in the SOI die may be implanted with a variety of dopants). Taking into consideration the ambiguous nature of the Examiner's questions, Appellant has attempted to answer the questions.

The Specification explains that the optical beam may be pulsed wherein the beam would be prevented from reaching the circuit when the optical beam is in the "off" mode of a pulse sequence. The optical signal would also not be detected when the optical beam is pulsed "off." The Examiner suggests that if the optical beam is prevented from reaching the circuit, the device would not be functional. Appellant is unsure to which "device" the Examiner is referring, and the Examiner fails to clarify. When the optical beam is pulsed "on" and "off," the testing arrangement is functional. *See* page 7, lines 11-14, of the instant Specification. If the optical beam is off for an extended period of time, the testing arrangement is not necessarily in an enabled and operational mode. If the "device" referred to is the integrated circuit (IC), the Specification discusses an IC device as a defective IC device and a non-defective IC device. *See id.* If the Examiner is referring to the IC device as the defective device, then the device is always non-functional; therefore, the issue as to when the beam is pulsed off is not relevant.

The Examiner also notes that carriers created by optical means will still be available for electrical interaction with the circuit. Appellant has questioned how carriers relate and whether the Examiner is attempting to ask this question in the context of a defective integrated circuit device or a non-defective circuit device. *See id.* Again, the Examiner fails

to clarify. Further, the Specification does not have to explain what may happen within particular aspects of circuitry since they are not claimed. MPEP § 2163. Despite the irrelevance of the Examiner's questions and conclusions regarding the claim language at issue, each of the questions and conclusions are believed to have been addressed and overcome. For these additional reasons, Appellant requests that the Section 112(2) rejection be reversed.

The Examiner's apparent concerns with the claim language at issue do not provide adequate grounds for a Section 112(2) rejection. A Section 112(2) inquiry during examination is the patentability of the invention as the applicant regards the invention. MPEP § 2171. Appellant has repeatedly clarified the claim language at issue, including examples from the instant Specification and extrinsic evidence. If the Examiner disagrees with Appellant's explanation of the instant invention, he should state the reasons of disagreement. Section 112(2) is not an appropriate statutory basis for rejecting Appellant's claims in view of the Examiner's apparent concerns, which have not been explained further. Appellant's claims particularly point out and distinctly claim that which Appellant regards as the invention, therefore the Section 112(2) rejection is improper.

**2. The Examiner's continued rejection of claims 12-20 under 35 U.S.C. § 112(2) improperly ignores the evidence of record.**

Appellant has repeatedly traversed the Section 112 rejection and addressed the Examiner's questions and conclusions, contrary to the assertion at page 3 of the final Office Action dated March 15, 2005. Appellant addressed the Examiner's claim-terminology concerns in each response: the Office Action Response filed on February 19, 2004, in the Office Action Response and Amendment After Final filed on June 28, 2004, in the Appeal Brief filed on September 22, 2004, in the Office Action Response filed on January 4, 2005, and in the Office Action Response After Final filed on May 16, 2005. Appellant first introduced evidence of the plain meaning of the term "inhibit" from the instant Specification and in the form of dictionary definitions as part of the arguments in the Office Action Response and Amendment After Final filed on June 28, 2004. In this second Appeal Brief, Appellant again traverses the rejection because the claimed language clearly points out the subject matter of the invention (as supported by the evidence of record) and the Examiner's

stated concerns with the claim language do not satisfy the requirements of a Section 112(2) rejection.

The sole evidence of record, including cited portions of the Specification and dictionary definitions, supports the plain meaning of the rejected claim terms as they are used to describe the instant invention. These terms concern the modulation of an optical beam being adapted to “inhibit optical beam intrusion upon the integrated circuit.” The MPEP requires that claim terms be read in view of their plain meaning when used in a manner consistent with the accepted meaning. *See* MPEP § 706.03(d). The sources for determining this meaning were recently identified by the Federal Circuit to be intrinsic sources such as the Specification and prosecution history as supplemented by extrinsic sources such as dictionaries. *Phillips v. AWH Corporation* (Nos. 03-1269, -1286; July 12, 2005). This questioned claim terminology was explained in the Office Action Response filed on February 19, 2004, in the Office Action Response and Amendment After Final filed on June 28, 2004, in the Appeal Brief filed on September 22, 2004, in the Office Action Response filed on January 4, 2005, and in the Office Action Response After Final filed on May 16, 2005. As supported by the instant Specification, *e.g.*, page 6, lines 14-20, and Figure 1, the modulated optical beam reaches the selected portion of the die and the modulation is used to inhibit the optical beam’s intrusion on the IC:

According to an example embodiment of the present invention, an optical beam is directed at a selected portion of a conventional flip chip type SOI die. The beam is pulsed at an interval that is sufficient to inhibit intrusion of the beam into the die. A reflected optical response from the SOI is obtained from the die and used to generate a waveform representing an electrical characteristic of the die. In this manner, analysis of SOI flip chip dies is made possible while maintaining minimal beam intrusion, and without necessarily destroying the die.

Also, the dictionary definition of “inhibit” is consistent with Appellant’s Specification: the Merriam-Webster online dictionary ([www.m-w.com](http://www.m-w.com)) defines “inhibit” as to hold in check, or restrain and the dictionary at [www.hyperdictionary.com](http://www.hyperdictionary.com) defines “inhibit” as to limit the range or extent of. As Appellant has explained that the claim term at issue is directed to an optical beam of short duration so as to limit intrusion on the integrated circuit, the rejection is based on an unsupported and irrelevant comment or opinion proffered by the Examiner. It would appear, as further discussed below, that the Examiner is attempting to

ignore important claim limitations in order to support the stated prior art rejection. Appellant submits that the Examiner has ignored the evidence of record and the Section 112(2) rejection is improper. Accordingly, Appellant requests that the Section 112(2) rejection be reversed.

**B. The Section 103(a) rejection of claims 12-16, 18 and 19 is generally improper and the Section 103(a) rejection of claim 15 is further deficient.**

**1. The rejection of claims 12-16, 18 and 19 is generally improper because the Examiner has failed to satisfy each of the three requirements of a *prima facie* Section 103(a) rejection.**

The Examiner has failed to satisfy each of the three requirements of a proper Section 103(a) rejection. In order to present a proper Section 103(a) rejection, the Examiner must present a combination of references that teaches or suggests each of the claimed limitations, present evidence of suggestion or motivation to combine the cited references, and have a reasonable expectation of success for the proposed combination. MPEP § 2143. Throughout the prosecution of this application, Appellant has shown that the Examiner has failed to satisfy any of these three criteria; therefore, the Section 103(a) rejection is improper and should be reversed.

**a. Cited References Fail to Correspond to the Claimed Invention**

The Examiner has failed to identify a combination of references that corresponds to the claimed invention and, more specifically, has failed to present any teachings in the cited references of a modulated beam adapted to inhibit optical beam intrusion upon an integrated circuit. *See* independent claims 12 and 13. While the Examiner alleges that the ‘179 reference teaches the alleged mode-locked laser modulation being used to inhibit optical beam intrusion upon the integrated circuit, Appellant fails recognize where this teaching exists. The Examiner has not cited any teachings in the ‘179 reference that would correspond to these claimed limitations. The ‘006 reference fails to compensate for this deficiency in the ‘179 teachings, as the ‘006 light is not modulated nor modulated so as to inhibit optical beam intrusion, as claimed. Without a showing of complete correspondence to each of the claimed limitations, the Section 103(a) rejection is improper and cannot be maintained. Appellant accordingly requests that the rejection be withdrawn.

Moreover, it would appear that the Examiner is employing a Section 112(2) rejection in an attempt to ignore certain of Appellant's claim language. As discussed above, Appellant has provided both an explanation and support to further clarify the claim language at issue. Thus the Section 112 rejection is improper and should not be used as a shield to ignore certain claim limitations. Correspondence must be shown to each of the claim limitations to sustain a Section 103(a) rejection and the Examiner has failed to satisfy this requirement.

b. No Evidence Has Been Provided to Combine the Cited References

The Examiner has failed to present evidence of motivation to combine the cited references to achieve the limitations of the present invention. The primary, '179, reference, as acknowledged by the Examiner, makes no mention of SOI structures. Therefore the '179 teachings fail to recognize problems associated specifically with SOI structures. The Examiner erroneously asserts that since the '006 reference teaches an optical technique for analyzing an SOI structure, "it would be obvious" to use the '179 optical technique for an SOI substrate because both SOI structures and the '179 substrates contain circuits. The optical techniques taught by the '179 and '006 references respectively are entirely different techniques that are not necessarily interchangeable to various devices and structures. The Examiner has not cited any teachings in the '179 reference that would suggest using the '179 optical techniques for SOI structures. Moreover, the Examiner fails to identify how the '179 teachings would be modified to address the specific problems associated with SOI structures, *e.g.*, optical beams disrupting or damaging circuitry components. Without a presentation of evidence from the cited teachings, that one skilled in the art would combine the cited teachings to achieve the limitations of the claimed invention, the Section 103(a) rejection is improper and should be withdrawn.

c. Proposed Combination is Destructive, Undermining Any Expectation of Success

Further, the Examiner should not have an expectation of success because the proposed modification would frustrate the purpose and operation of the '179 teachings thereby rendering the proposed modification unmotivated and improper. The MPEP states that when a proposed modification would render the teachings being modified unsatisfactory

for their intended purpose, there is no suggestion or motivation to make the proposed modification under 35 U.S.C. § 103(a). *See* MPEP § 2143.01. The Examiner suggests inserting the damaged ‘006 substrate (substrate has pin holes in the buried oxide layer as shown in Figures 1, 4 and 5) or the damaging analysis technique of the ‘006 teachings into the ‘179 teachings. The ‘179 reference is directed to operating a DUT to detect electrical waveforms corresponding to varying voltages. *See* col. 7, line 65 – col. 8, line 2. The damaged ‘006 substrate would not operate properly while under test to provide the desired voltage correlation data. Moreover, the ‘179 backside analysis technique would result in the mode-locked laser intruding into the SOI circuitry thereby disrupting the operation of the structure and likely damaging the circuitry, thus eliminating the possibility of testing the structure’s integrity. To suggest that the skilled artisan would use the ‘179 teachings on the ‘006 SOI structure is untenable and would undermine the purpose and operation of the ‘179 reference. Thus, the proposed combination is unmotivated and Appellant requests that the Section 103(a) rejection be reversed.

**2. The Section 103(a) rejection of claim 15 is improper because the Examiner ignores claim limitations directed to the optical beam pulse length.**

With particular respect to claim 15, the Section 103(a) rejection is improper because the proposed combination fails to correspond to each of the claimed limitations. Ignoring Appellant’s arguments, the Examiner has concluded that “[t]here is no evidence that pulse length is critical.” Claim 15 is specifically directed to an optical beam arrangement adapted to pulse a laser at “femto-second-range pulses,” with the modulation being important for a circuit structure problem that is not a concern for the ‘179 reference. The import of the claimed pulse length is specifically discussed at page 7, lines 8-11: “The femto-second pulse duration aids in analysis of circuitry operating at high frequency, and in circuitry located such that analysis using a laser having a longer pulse or constant application would harm the die.” The Examiner cannot ignore such specific claim limitations when none of the cited references recognize or address the problem. *See* MPEP § 2141.02. This is part of the “subject matter as a whole” which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103. Without a showing of correspondence to

each of the claimed limitations, the Section 103(a) rejection cannot stand and Appellant requests that the rejection be reversed.

**C. The Section 103(a) rejection of dependent claims 17 and 20 is improper because the Examiner fails to satisfy any of the three requirements for a Section 103(a) rejection as shown with respect to the underlying independent claims.**

The rejection of dependent claims 17 and 20 is improper for the reasons discussed above in connection with independent claims 12 and 13. The rejection of claims 17 and 20 relies upon the same primary combination of the '179 reference with the '006 reference that is shown to be insufficient grounds of rejection as discussed above. "If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Thus, the rejection of dependent claims 17 and 20 under 35 U.S.C. § 103 should be reversed.

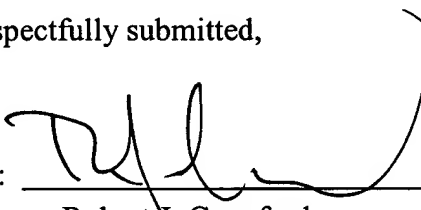
**VIII. Conclusion**

In view of the above, Appellant submits that the rejections are improper, the claimed invention is patentable, and that the rejections of claims 12-20 should be reversed. Appellant respectfully requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

CRAWFORD MAUNU PLLC  
1270 Northland Drive – Suite 390  
St. Paul, MN 55120  
(651) 686-6633

Respectfully submitted,

By:   
Name: Robert J. Crawford  
Reg. No. 32,122

## **APPENDIX OF APPEALED CLAIMS**

12. An arrangement for analyzing an integrated circuit having a silicon on insulator (SOI) structure, the arrangement comprising;

means for directing a modulated optical beam at a selected portion of the SOI structure, the modulation being adapted to inhibit optical beam intrusion upon the integrated circuit; and

means for obtaining a reflected optical waveform response from the SOI selected portion.

13. A system for analyzing an integrated circuit having a silicon on insulator (SOI) structure, the system comprising;

an optical beam arrangement adapted to direct a modulated optical beam at a selected portion of the SOI structure and to inhibit intrusion of the optical beam upon the integrated circuit via the modulation; and

a detection arrangement adapted to detect a reflected optical waveform response from the SOI structure selected portion.

14. The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 13, wherein the optical beam arrangement includes an infrared laser.

15. The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 14, wherein the optical beam arrangement is adapted to pulse the laser at femto-second-range pulses.

16. The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 14, further comprising a testing device adapted to operate the die.

17. The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 13, further comprising a computer arrangement coupled to the detector arrangement and adapted to receive and process the reflected optical waveform response.

18. The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 17, further comprising a visual output arrangement coupled to the computer arrangement and adapted to present data from the computer arrangement for visual analysis.

19. The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 18, wherein the visual output arrangement includes at least one of: a video monitor and a printer.

20. (original) The system for analyzing an integrated circuit having a silicon on insulator (SOI) structure of claim 19, wherein the computer arrangement includes waveform analysis software.

## **EVIDENCE APPENDIX**

None.

## **RELATED PROCEEDINGS APPENDIX**

None.